500.43581X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	AKIYAMA
Application No.:	10/790,880
Filed:	3/3/2004
Title:	SEMICONDUCTOR DEVICE
Art Unit:	2188
Exr.:	D. TRAN **CONF. No.: 4729**

STATEMENT OF SUBSTANCE OF INTERVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 10, 2008

Sir:

Appreciation is expressed to Exr. Denise Tran for her courtesy and helpfulness during a telephone interview conducted in the above matter on November 7, 2008. During the course of the telephone interview, Exr. Tran reviewed the amendments to claim 1 in the amendment filed on November 5, 2008 and advised the undersigned attorney that, although it appeared that these amendments might overcome the present prior art of record, substantial further review of the prior art of record would be required to confirm that this was, in fact, the case. Further, Exr. Tran advised the undersigned attorney that it would also be necessary to conduct a further search of this matter, even if she confirmed her conclusion of distinguishing over the prior art, to determine whether other pertinent prior art might exist regarding the amended claims. Accordingly, Exr. Tran advised the undersigned attorney that it would be required to file an RCE to obtain full consideration of the November 5, 2008 Amendment. Therefore, the present RCE is being filed to obtain full consideration with Exr. Tran's conclusion regarding this matter.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

By /Gregory E. Montone/
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Response Under 37 CFR §1.116
Expedited Procedure

500.43581X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: AKIYAMA et al

Serial No.: 10/790,880

Filed: March 3, 2004

For: Semiconductor Device

Art Unit: 2185

Examiner: D. Tran **CONF. No. 4729**

Notice of Appeal Filed November 8, 2008

AMENDMENT AFTER FINAL REJECTION
UNDER 37 CFR §1.116

Mail Stop: Amendment After Final
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 5, 2008

Sir:

In response to the Final Office Action dated April 7, 2008, noting that the time for response has been extended by the filing of a Notice of Appeal and a Petition for Extension of Time on November 8, 2008, and under the provisions of 37 CFR §1.116, please amend the above-identified application as listed below and set forth on the following pages:

Amendments to the Claims; and

Remarks are included following the amendments.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation; and

a cache memory for mediating an access to said plurality of memory banks from the outside,

said cache memory having a number of ~~way~~ ways equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells;

wherein, when first data is written into said semiconductor device from the outside, and when said cache memory does not hold an address at which said first data is to be written, data held in an associated entry of said cache memory is written back to one of said plurality of memory banks, and said first data is written into said cache memory, and

wherein, when data is written back to one of said plurality of memory banks, and when a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks.

2. (original) A semiconductor device according to claim 1, wherein:

said cache memory has a plurality of sets corresponding to the number of ways, and

each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks.

3. (original) A semiconductor device according to claim 1, wherein:

when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory.

Claim 4 (canceled).

Claim 5 (Canceled).

6. (original) A semiconductor device according to claim 1, further comprising:

a plurality of data input/output nodes for inputting/outputting data to/from the outside,

wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device.

7. (original) A semiconductor device according to claim 1, further comprising:

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line comprised of a plurality of sublines, and

$$A = N \cdot B$$

is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus.

8. (original) A semiconductor device according to claim 7, wherein:

said cache memory has a plurality of flags each associated with one subline for managing data held thereon; and

when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank.

9. (Previously Presented) A semiconductor device according to claim 7, wherein:

when a flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory.

10. (original) A semiconductor device according to claim 1, wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell.

11. (original) A semiconductor device according to claim 10, wherein said cache memory comprises SRAM memory cells.

12. (original) A semiconductor device according to claim 1, wherein said cache memory comprises SRAM memory cells.

Claims 13 through 19 (canceled).

20. (Currently Amended) A semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation; and

a cache memory for mediating an access to said plurality of memory banks from the outside,

said cache memory having a number of ways equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read

cycle (n) of said memory cells;

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line comprised of a plurality of sublines, and

$A = N \cdot B$

is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus,

wherein, when data is written back to one of said plurality of memory banks, and when a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks.

21. (Previously Presented) A semiconductor device according to claim 20, wherein:

said cache memory has a plurality of sets corresponding to the number of ways, and

each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks.

22. (Previously Presented)A semiconductor device according to claim 20, wherein:

when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory.

23. (Previously Presented) A semiconductor device according to claim 20, further comprising:

a plurality of data input/output nodes for inputting/outputting data to/from the outside,

wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device.

24. (Previously Presented) A semiconductor device according to claim 20, wherein:

said cache memory has a plurality of flags each associated with one subline for managing data held thereon; and

when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank.

25. (Previously Presented) A semiconductor device according to claim 20, wherein:

when a flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory.

26. (Previously Presented) A semiconductor device according to claim 20, wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell.

27. (Previously Presented) A semiconductor device according to claim 26, wherein said cache memory comprises SRAM memory cells.

28.(Previously Presented) A semiconductor device according to claim 20, wherein said cache memory comprises SRAM memory cells.

REMARKS

Entry of this amendment, and reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the final Office Action dated April 7, 2008. By the present amendment, the claims have been amended to clarify the distinctions over the primary reference to Akiyama (USPub. 2003/0033492), which is the primary reference in the 35 USC §103 rejection. Accordingly, reconsideration and removal of that rejection is requested for the reasons set forth below.

Specifically, by the present amendment, the claims have been amended to particularly define that when data written back to a first memory bank cannot be accepted by the first memory bank due to a write operation, the data is written back to a second memory bank which is different than the first memory bank. It is respectfully submitted that the amendment clearly defines the difference of the present invention from the arrangement taught by Akiyama, as will be discussed below.

With regard to Akiyama, the last paragraph of the independent claims 1 and 20 (now amended) has been indicated as being readable on paragraph [0058] of the Akiyama reference. In other words, the Office Action states that the claimed feature of writing data back to a second memory bank rather than the first memory bank, when the first memory bank cannot accept an access from the outside, is met by paragraph [0058] of Akiyama. It is respectfully submitted that a careful review of paragraph [0058] of Akiyama, particularly as amended, clearly leads to the

conclusion that the operation of Akiyama is completely different than that defined by the amended claim.

In particular, paragraph [0058] of Akiyama defines the feature of that patent that when there is invalid data in the entry at a cache miss, the invalid data will not be written back but, instead, other data will be written back to write data "e" of bank 8 into the entry, irrespective as to whether the bank 8 is accessible (e.g., refreshed) or not. As such, there is no teaching of writing data back to a second memory bank, different from the first memory bank, when the first memory bank cannot accept access from the outside. Further, it is respectfully submitted that there is absolutely nothing that Akiyama teaches that would lead one to write data back to a second memory bank, rather than a first memory bank, when the reason that the first memory bank cannot accept the access from the outside is due to a write operation. With regard to this, it is noted that in Akiyama, the bank 4 is a bank to be written back, and invalid data is not written in the write back operation at bank 4. As such, there is nothing in Akiyama which teaches writing data back to a different memory bank when a first memory bank cannot accept an access from the outside due to a write operation.

By virtue of these amendments to the independent claims, it is respectfully submitted that the distinction of the present invention over Akiyama is clearly set forth. Further, it is respectfully submitted that nothing in the secondary cited references makes us for this shortcoming in the primary reference to Akiyama in meeting the prior art. Therefore, reconsideration and removal of the prior art rejection based on Akiyama is earnestly solicited.

Entry of this amendment is respectfully requested, notwithstanding the finality of the Office Action. With regard to this, it is respectfully submitted that the present amendment is directed to clarification of features already argued with regard to the

claims. In other words, the claims are amended to more clearly correlate the claim language with features previously argued and considered by the Examiner. For example, on page 7 of the Office Action, the Examiner specifically refers to paragraph [0058] concerning the requested address and the writing back of data back to the bank 4. The present amendment clarifies the distinction over this point raised in the Office Action by emphasizing that the reason that the first memory bank cannot accept the access is due to a write operation, and, in such an instance, the data is written back to a second different memory bank from the first memory bank that cannot accept the access. Since the Examiner has apparently already considered and searched for writing back data when a memory bank cannot accept an access, it is respectfully submitted that the clarifying amendment should not require further search or substantial consideration by the Examiner. Further, it is respectfully submitted, that these distinguishing amendments should place the application in condition for allowance or, at a minimum, clarify the issues for appeal. Therefore, entry of this amendment either for purposes of placing the application in condition for allowance or clarifying the issues for appeal is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus,

LLP Deposit Account No. 01-2135 (Docket No. 500.43581X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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